IN THE CLAIMS:

1. (Currently Amended) An apparatus comprising:

an amplifier;

a first inverter having an input coupled to an output of the amplifier; and

a second inverter having an input coupled to an output of the first inverter and an output, wherein the output of the second inverter is fed back to an input of the amplifier;

wherein the amplifier provides positive feedback and the output of the second inverter is fed back to the amplifier as negative feedback; and

wherein the amplifier mixes the positive feedback and the negative feedback.

2. (Original) The apparatus as claimed in claim 1, wherein the amplifier is a CMOS amplifier.

3. (Original) The apparatus as claimed in claim 2, wherein the CMOS amplifier is a hybrid Bazes and Chappell amplifier.

4. (Currently Amended) The apparatus as claimed in claim 3, wherein:

the amplifier includes a first, a second and a third pMOS transistor and a first, a second and a third nMOS transistor;

a gate of the first pMOS transistor and a gate of the first nMOS transistor are coupled to an input;

a gate of the second pMOS transistor and a gate of the ~~first~~ second nMOS transistor are coupled to a drain of the first pMOS transistor and a drain of the first nMOS transistor; and

a gate of the third pMOS transistor and a gate of the third nMOS transistor are coupled to an inverse input.

5. (Currently Amended) The apparatus as claimed in claim 4, wherein the gate of the second pMOS transistor and the gate of the ~~first~~ second nMOS transistor are coupled to the drain of the first pMOS transistor and the drain of the first nMOS transistor via a resistor.

6. (Original) The apparatus as claimed in claim 1, wherein the second inverter is approximately four times the size of the first inverter.

7. (Original) The apparatus as claimed in claim 1, wherein the first inverter is approximately one-fourth the size of the output of the amplifier.

8. (Original) The apparatus as claimed in claim 1, wherein the first inverter is approximately one-fourth the size of the output of the amplifier and the first inverter is approximately one-fourth the size of the second inverter.

9. (Original) The apparatus as claimed in claim 1, wherein the output of the second inverter is fed back to the amplifier as negative feedback.

10. (Original) The apparatus as claimed in claim 1, wherein the amplifier provides positive feedback.

11. (Cancelled)

12. (Cancelled)

13. (Original) The apparatus as claimed in claim 4, wherein the amplifier further includes a resistor, wherein the resistor is included in a circuit that mixes positive feedback provided by the amplifier and negative feedback provided to the amplifier from the output of the second inverter.

14. (Original) The apparatus as claimed in claim 1, further comprising an output, wherein the output is coupled to the output of the second inverter.

15. (Original) The apparatus as claimed in claim 1, wherein the output does not include ~~precharge artifacts~~ evidence of precharging from the amplifier.

16. (Currently Amended) An apparatus comprising:

an amplifier; and

a delay and gain circuit coupled to an output of the amplifier, wherein an output of the delay and gain circuit is fed back to the amplifier;

wherein the amplifier provides positive feedback and the output of the delay and gain circuit is fed back to the amplifier as negative feedback; and

wherein the amplifier mixes the positive feedback and the negative feedback.

17. (Original) The apparatus as claimed in claim 16, wherein the output of the delay and gain circuit is fed back to the amplifier as negative feedback.

18. (Original) The apparatus as claimed in claim 16, wherein the amplifier provides positive feedback.

19. (Cancelled)

20. (Cancelled)

21. (Amended) The apparatus as claimed in claim ~~19~~ 16, wherein the amplifier includes a resistor, wherein the resistor is included in a circuit that mixes the positive feedback and the negative feedback.

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)

28-56 (Previously Cancelled)

57. (Previously Added) The apparatus as claimed in claim 1, the amplifier further comprising:

an inverse input;

a first pMOS transistor having a gate coupled to the input of the amplifier;

a second pMOS transistor;

a third pMOS transistor having a gate coupled to the inverse input of the amplifier and having a source coupled to a source of the first pMOS transistor and to a drain of the second pMOS transistor;

a first nMOS transistor having a gate coupled to the input of the amplifier;

a second nMOS transistor having a gate coupled to a drain of the first pMOS transistor, a drain of the first nMOS transistor, and to a gate of the second pMOS transistor; and

a third nMOS transistor having a gate coupled to the inverse input of the amplifier, a drain coupled to a drain of the third pMOS transistor and a source coupled to a source of the first nMOS transistor and to a drain of the second nMOS transistor, wherein the output of the amplifier is coupled to the drain of the third pMOS transistor and to the drain of the third nMOS transistor.

58. (Previously Added) The apparatus as claimed in claim 57, the amplifier further comprising a resistor, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled directly together, and the drain of the first pMOS transistor and the drain of the first nMOS transistor are coupled directly together, wherein the direct coupling of the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled via the resistor to the direct coupling of the drain of the first pMOS transistor and the drain of the first nMOS transistor.

59. (Previously Added) The apparatus according to claim 58, wherein the resistor has a resistance of approximately 5000 ohms.

60. (Previously Added) The apparatus according to claim 57, the amplifier further comprising a control input, wherein the gate of the second nMOS

transistor and the gate of the second pMOS transistor are coupled to the control input.

61. (Previously Added) The apparatus according to claim 57, wherein a width of each of the first pMOS transistor, the second pMOS transistor and the third pMOS transistor is approximately 9.2um, and wherein a width of the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 4um.

62. (Previously Added) The apparatus according to claim 61, wherein a length of each of the first pMOS transistor, the second pMOS transistor, the third pMOS transistor, the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 80nm.

63. (Previously Added) The apparatus as claimed in claim 16, the amplifier further comprising:

an input;

an inverse input;

a first pMOS transistor having a gate coupled to the input of the amplifier;

a second pMOS transistor;

a third pMOS transistor having a gate coupled to the inverse input of the amplifier and having a source coupled to a source of the first pMOS transistor and to a drain of the second pMOS transistor;

a first nMOS transistor having a gate coupled to the input of the amplifier;

a second nMOS transistor having a gate coupled to a drain of the first pMOS transistor, a drain of the first nMOS transistor, and to a gate of the second pMOS transistor; and

a third nMOS transistor having a gate coupled to the inverse input of the amplifier, a drain coupled to a drain of the third pMOS transistor and a source coupled to a source of the first nMOS transistor and to a drain of the second nMOS transistor, wherein the output of the amplifier is coupled to the drain of the third pMOS transistor and to the drain of the third nMOS transistor.

64. (Previously Added) The apparatus as claimed in claim 63, the amplifier further comprising a resistor, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled directly together, and the drain of the first pMOS transistor and the drain of the first nMOS transistor are coupled directly together, wherein the direct coupling of the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled via the resistor to the direct coupling of the drain of the first pMOS transistor and the drain of the first nMOS transistor.

65. (Previously Added) The apparatus according to claim 64, wherein the resistor has a resistance of approximately 5000 ohms.

66. (Previously Added) The apparatus according to claim 63, the amplifier further comprising a control input, wherein the gate of the second nMOS

transistor and the gate of the second pMOS transistor are coupled to the control input.

67. (Previously Added) The apparatus according to claim 63, wherein a width of each of the first pMOS transistor, the second pMOS transistor and the third pMOS transistor is approximately 9.2um, and wherein a width of the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 4um.

68. (Previously Added) The apparatus according to claim 67, wherein a length of each of the first pMOS transistor, the second pMOS transistor, the third pMOS transistor, the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 80nm.

69. (New) An apparatus comprising:

an amplifier;

a first inverter having an input coupled to an output of the amplifier; and

a second inverter having an input coupled to an output of the first inverter and an output, wherein the output of the second inverter is fed back to an input of the amplifier;

wherein:

the CMOS amplifier is a hybrid Bazes and Chappell amplifier;

the amplifier includes a first, a second and a third pMOS transistor and a first, a second and a third nMOS transistor;

a gate of the first pMOS transistor and a gate of the first nMOS transistor are coupled to an input;

a gate of the second pMOS transistor and a gate of the second nMOS transistor are coupled to a drain of the first pMOS transistor and a drain of the first nMOS transistor;

a gate of the third pMOS transistor and a gate of the third nMOS transistor are coupled to an inverse input; and

the amplifier further includes a resistor, wherein the resistor is included in a circuit that mixes positive feedback provided by the amplifier and negative feedback provided to the amplifier from the output of the second inverter.

70. (New) The apparatus as claimed in claim 69, wherein the amplifier is a CMOS amplifier.

71. (New) The apparatus as claimed in claim 69, wherein the gate of the second pMOS transistor and the gate of the second nMOS transistor are coupled to the drain of the first pMOS transistor and the drain of the first nMOS transistor via a resistor.

72. (New) The apparatus as claimed in claim 69, wherein the second inverter is approximately four times the size of the first inverter.

73. (New) The apparatus as claimed in claim 69, wherein the first inverter is approximately one-fourth the size of the output of the amplifier.

74. (New) The apparatus as claimed in claim 69, wherein the first inverter is approximately one-fourth the size of the output of the amplifier and the first inverter is approximately one-fourth the size of the second inverter.

75. (New) The apparatus as claimed in claim 69, wherein the output of the second inverter is fed back to the amplifier as negative feedback.

76. (New) The apparatus as claimed in claim 69, wherein the amplifier provides positive feedback.

77. (New) The apparatus as claimed in claim 69, wherein the amplifier provides positive feedback and the output of the second inverter is fed back to the amplifier as negative feedback.

78. (New) The apparatus as claimed in claim 77, wherein the amplifier mixes the positive feedback and the negative feedback.

79. (New) The apparatus as claimed in claim 69, further comprising an output, wherein the output is coupled to the output of the second inverter.

80. (New) The apparatus as claimed in claim 69, wherein the output does not include precharge artifacts from the amplifier.

81. (New) The apparatus as claimed in claim 69, the amplifier further comprising:

an inverse input;

a first pMOS transistor having a gate coupled to the input of the amplifier;

a second pMOS transistor;

a third pMOS transistor having a gate coupled to the inverse input of the amplifier and having a source coupled to a source of the first pMOS transistor and to a drain of the second pMOS transistor;

a first nMOS transistor having a gate coupled to the input of the amplifier;

a second nMOS transistor having a gate coupled to a drain of the first pMOS transistor, a drain of the first nMOS transistor, and to a gate of the second pMOS transistor; and

a third nMOS transistor having a gate coupled to the inverse input of the amplifier, a drain coupled to a drain of the third pMOS transistor and a source coupled to a source of the first nMOS transistor and to a drain of the second nMOS transistor, wherein the output of the amplifier is coupled to the drain of the third pMOS transistor and to the drain of the third nMOS transistor.

82. (New) The apparatus as claimed in claim 81, the amplifier further comprising a resistor, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled directly together, and the drain of the first pMOS transistor and the drain of the first nMOS transistor are coupled directly together, wherein the direct coupling of the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled via the resistor to the direct coupling of the drain of the first pMOS transistor and the drain of the first nMOS transistor.

83. (New) The apparatus according to claim 82, wherein the resistor has a resistance of approximately 5000 ohms.

84. (New) The apparatus according to claim 81, the amplifier further comprising a control input, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled to the control input.

85. (New) The apparatus according to claim 81, wherein a width of each of the first pMOS transistor, the second pMOS transistor and the third pMOS transistor is approximately 9.2um, and wherein a width of the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 4um.

86. (New) The apparatus according to claim 85, wherein a length of each of the first pMOS transistor, the second pMOS transistor, the third pMOS transistor, the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 80nm.